CJC5340

100dB, 192 kHz, Multi-Bit Audio A/D Converter

Edition	Author	Date	Description
V1.1	By tf	2011.09	101 dB, 192 KHz, Multi-Bit Audio A/D Converter
V1.2	By tf	2011.12	Properties updata

Features

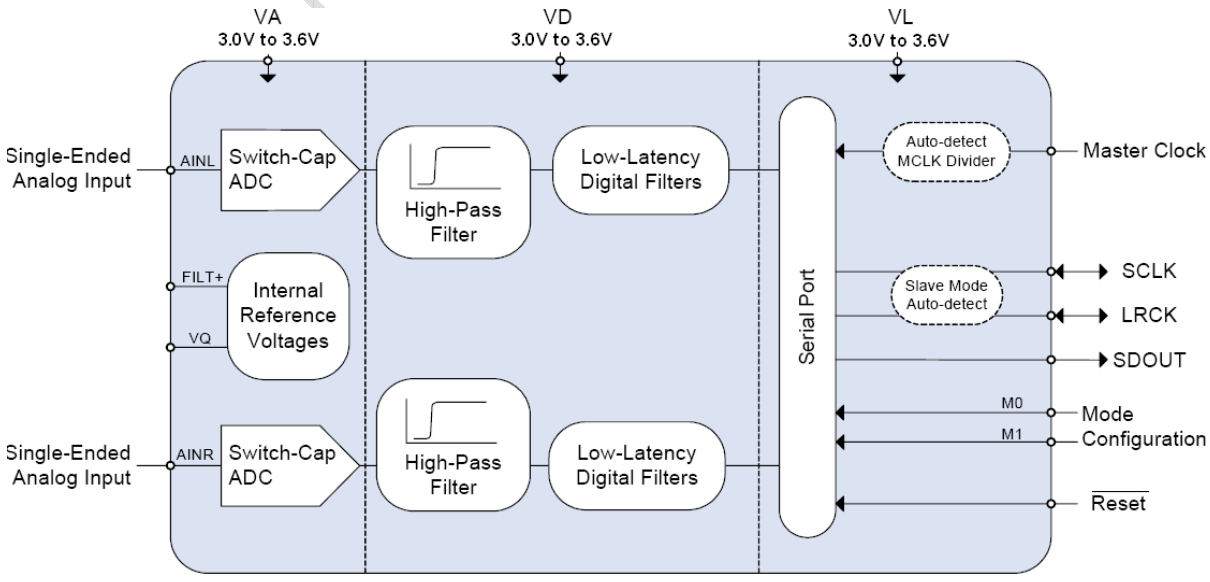
- Advanced Multi-bit Delta-Sigma Architecture
- 24-bit Conversion
- Supports All Audio Sample Rates Including 192 kHz
- -88 dB THD+N
- 77 mW Power Consumption
- High-Pass Filter to Remove DC Offsets
- Analog/Digital Core Supplies from 3 V to 3.6V
- Supports Logic Levels from 3 V to 3.6 V
- Auto-detect Mode Selection in Slave Mode
- Auto-Detect MCLK Divider

General Description

The CJC5340 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering, generating 24-bit values for both left and right inputs in serial format sample rates up to 200 kHz per channel.

The CJC5340 uses a 5th-order, multi-bit Delta-Sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The CJC5340 is available in a 16-pin TSSOP package for Commercial (-10° to +70° C) and Automotive grades (-40° to +85° C).

The CJC5340 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as set-top boxes, DVD-karaoke players, DVD recorders, A/V receivers, and automotive applications.



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CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and TA = 25° C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Analog	VA	3	3.3	3.6	V
	Digital	VD	3	3.3	3.6	V
	Logic	VL	3	3.3	3.6	V
Ambient Operating Temperature	Commercial	TAC	-10		70	℃
	Automotive	TAC	-40		85	℃

Notes:

1. This part is specified at typical analog voltages of 3 V and 3.6 V. See Analog Characteristics – Commercial Grade and Analog Characteristics - Automotive Grade, below, for details.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 2)

Parameter		Symbol	Min	Max	Units
DC Power Supplies: Analog Logic Digital		VA	-0.3	+3.6	V
		VL	-0.3	+3.6	V
		VD	-0.3	+3.6	V
Input Current	(Note 3)	Iin	-10	+10	mA
Analog Input Voltage	(Note 4)	VIN	GND-0.7	VA+0.7	V
Digital Input Voltage	(Note 4)	VIND	-0.7	VL+0.7	V
Ambient Operating Temperature (Power Applied)		TA	-50	+95	℃
Storage Temperature		Tstg	-65	+150	℃

2. Operation beyond these limits may result in permanent damage to the device.Normal operation is not guaranteed at these extremes.

3. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

4. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS - COMMERCIAL GRADE

Test Conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Dynamic Performance for Commercial Grade		VA = 3.3 V			
Single-Speed Mode Fs = 48 kHz	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range A-weighted			**96**		**dB**
Total Harmonic Distortion + Noise (Note 5) -1 dB	**THD+N**		**87**		**dB**
Double-Speed Mode Fs = 96 kHz	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Dynamic Range A-weighted			**96**		**dB**
Total Harmonic Distortion + Noise (Note 5) -1 dB	**THD+N**		**84**		**dB**
Dynamic Performance All Modes		**Min**	**Typ**	**Max**	**Unit**
Interchannel Isolation			**92**		**dB**
Analog Input Characteristics					
Full-Scale Input Voltage			**0.56*VA**		**mV**

5. Referred to the typical full-scale input voltage

DIGITAL FILTER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode					
Passband (-0.1 dB) (Note 6)		0	-	0.4895	Fs
Passband Ripple		-0.035	-	0.035	dB
Stopband (Note 6)		0.5687	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	tgd	-	12/Fs	-	s
Double-Speed Mode					
Passband (-0.1 dB) (Note 6)		0	-	0.4895	Fs
Passband Ripple		-0.025	-	0.025	dB
Stopband (Note 6)		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	tgd	-	9/Fs	-	s
Quad-Speed Mode					
Passband (-0.1 dB) (Note 6)		0	-	0.2604	Fs
Passband Ripple		-0.025	-	0.025	dB
Stopband (Note 6)		0.5	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	tgd	-	5/Fs	-	s
High-Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 7)		-	20	-	Hz
Phase Deviation @ 20 Hz (Note 7)		-	10	-	Deg
Passband Ripple		-	-	0	dB

6. Filter characteristics scale precisely with Fs

7. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

DC ELECTRICAL CHARACTERISTICS

(GND = 0 V, all voltages with respect to 0 V. MCLK=12.288 MHz; Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies: Positive Analog		VA	3	3.3	3.6	V
Positive Digital		VD	3	3.3	3.6	V
Positive Logic		VL	3	3.3	3.6	V
(Normal Operation)	VA = 3.3 V	IA	17.2	17.36	18.1	mA
	VD = 3.3 V	ID	1.16	1.26	2.2	mA
	VL = 3.3 V	IL	0.43	0.97	1.06	mA
Power Supply Rejection Ratio (1 kHz)	(Note 8)	PSRR		50		dB

8. Power Down Mode is defined as RST = Low, with all clocks and data lines held static at a valid logic levels.

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	(% of VL)	VIH	70%	-	-	V
Low-Level Input Voltage	(% of VL)	VIL	-	-	30%	V
High-Level Output Voltage at Io = 100	A (% of VL)	VOH	70%	-	-	V
Low-Level Output Voltage at Io =100	A (% of VL)	VOL	-	-	15%	V
Input Leakage Current		Iin	-10	-	10	A

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic "0" = GND = 0 V; Logic "1" = VL, CL = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Specifications					
MCLK Period	tclkw	39	-	45	ns
		78	-	1953	ns
MCLK Pulse Duty Cycle		40	-	60	%
Master Mode					
SCLK falling to LRCK Single-Speed	tmslr	-20	-	20	ns
Double-Speed		-20	-	20	ns
Quad-Speed		-8	-	8	ns
SCLK falling to SDOUT valid.	tsdo	-	-	32	ns
SCLK Duty Cycle. Single-Speed		-	50	-	%
Double-Speed		-	50	-	%
Quad-Speed		-	30	-	%
Slave Mode					
Single-Speed (Note 9)					
LRCK Duty Cycle		40	50	60	%
SCLK Period	tsclkw	156	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	tstp	10	-	-	ns
SDOUT valid after SCLK rising	thld	5	-	-	ns
SCLK falling to LRCK edge	tslrd	-20		20	ns
Double-Speed (Note 9)					
LRCK Duty Cycle		40	50	60	%
SCLK Period	tsclkw	156	-	-	ns
SCLK Duty Cycle		45	50	55	%
SDOUT valid before SCLK rising	tstp	10	-	-	ns
SDOUT valid after SCLK rising	thld	5	-	-	ns
SCLK falling to LRCK edge	tslrd	-20		20	ns
Quad-Speed (Note 9)					
LRCK Duty Cycle		40	50	60	%
SCLK Period	tsclkw	78	-	-	ns
SCLK Duty Cycle		29.7	33	50	%
SDOUT valid before SCLK rising	tstp	10	-	-	ns
SDOUT valid after SCLK rising	thld	5	-	-	ns
SCLK falling to LRCK edge	tslrd	-8		8	ns

9. For a description of speed modes, please refer to Table on page 15.

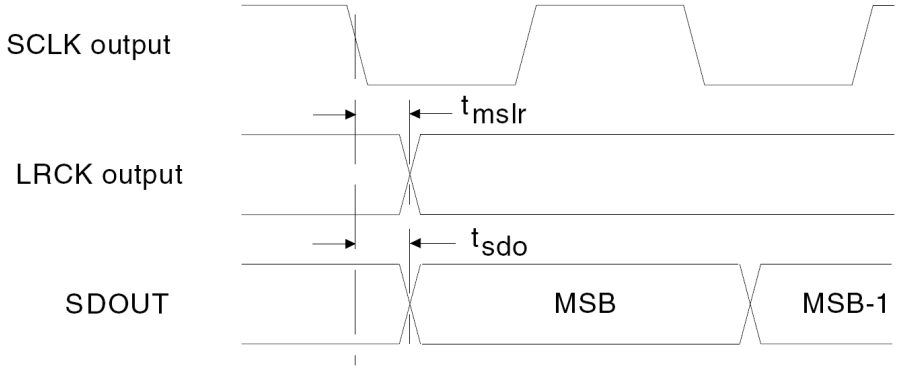


Figure 13. Master Mode, Left-Justified SAI

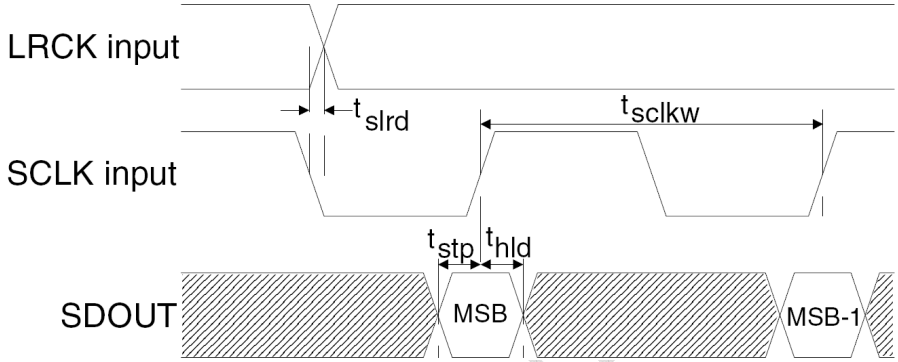


Figure 14. Slave Mode, Left-Justified SAI

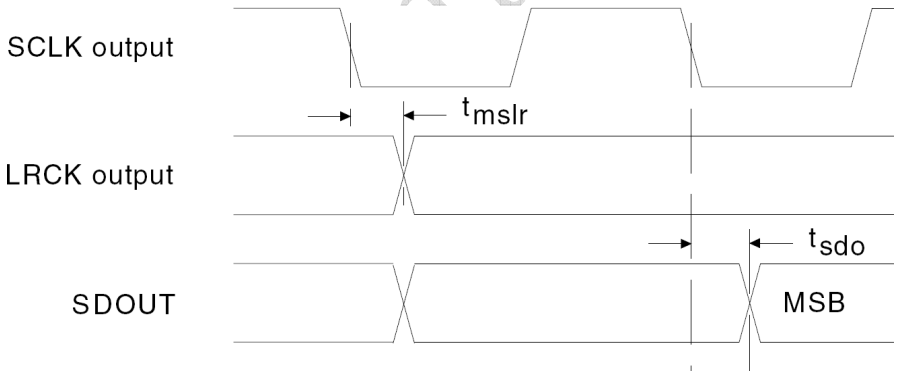


Figure 15. Master Mode, I²S SAI

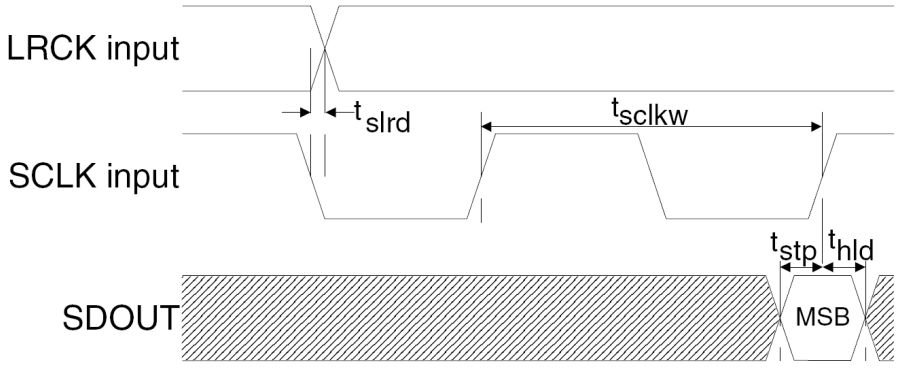
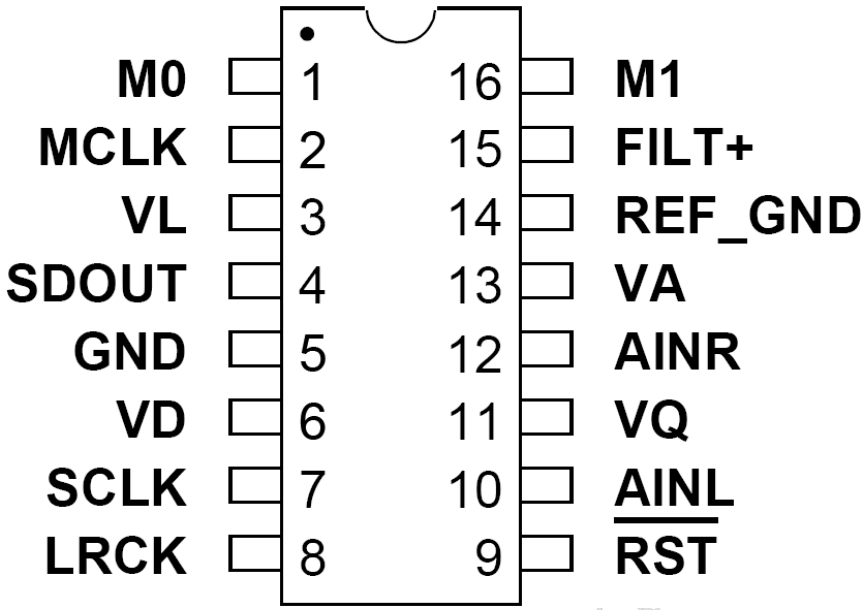


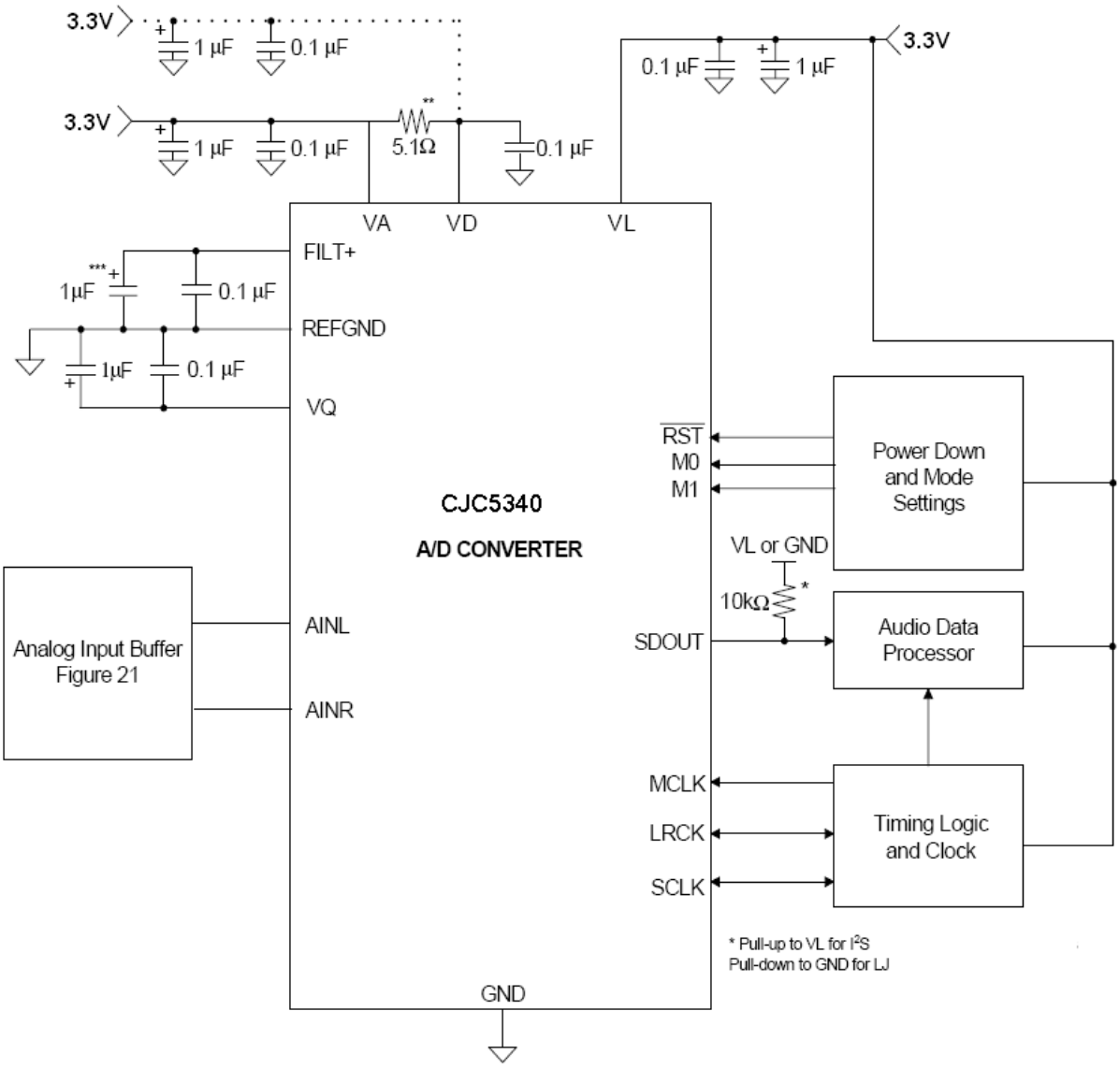
Figure 16. Slave Mode, I²S SAI

PIN DESCRIPTION



Pin Name	#	Pin Description
M0	1	**Mode Selection** (Input) - Determines the operational mode of the device.
M1	16	
MCLK	2	**Master Clock** (Input) - Clock source for the delta-sigma modulator and digital filters.
VL	3	**Logic Power** (Input) - Positive power for the digital input/output.
SDOUT	4	**Serial Audio Data Output** (Output) - Output for two's complement serial audio data.
GND	5,14	**Ground** (Input) - Ground reference. Must be connected to analog ground.
VD	6	**Digital Power** (Input) - Positive power supply for the digital section.
SCLK	7	**Serial Clock** (Input/Output) - Serial clock for the serial audio interface.
LRCK	8	**Left Right Clock** (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
/RST	9	**Reset** (Input) - The device enters a low power mode when low.
AINL	10	**Analog Input** (Input) - The full-scale analog input level is specified in the Analog Characteristics specification table.
AINR	12	
VQ	11	**Quiescent Voltage** (Output) - Filter connection for the internal quiescent reference voltage.
VA	13	**Analog Power** (Input) - Positive power supply for the analog section.
FILT+	15	**Positive Voltage Reference** (Output) - Positive reference voltage for the internal sampling circuits.

TYPICAL CONNECTION DIAGRAM



APPLICATIONS

Single-, Double-, and Quad-Speed Modes

The CJC5340 can support output sample rates from 2 kHz to 200 kHz. The proper speed mode can be determined by the desired output sample rate and the external MCLK/LRCK ratio, as shown in Table 1.

Speed Mode	MCLK/LRCK Ratio	Output Sample Rate Range (kHz)
Single-Speed Mode	512x	43 - 50
	256x	2 - 50
Double-Speed Mode	256x	86 - 100
	128x	4 - 100
Quad-Speed Mode	128x	172 - 200
	64x*	100 - 200
* Quad-Speed Mode, 64x only available in Master Mode.		

Table 1. Speed Modes and the Associated Output Sample Rates (Fs)

Operation as Either a Clock Master or Slave

The CJC5340 supports operation as either a clock master or slave. As a clock master, the LRCK and SCLK pins are outputs with the left/right and serial clocks synchronously generated on-chip. As a clock slave, the LRCK and SCLK pins are inputs and require the left/right and serial clocks to be externally generated. The selection of clock master or slave is made via the Mode pins as shown in Table 2.

M1 (Pin 16)	M0 (Pin 1)	MODE
0	0	Clock Master, Single-Speed Mode
0	1	Clock Master, Double-Speed Mode
1	0	Clock Master, Quad-Speed Mode
1	1	Clock Slave, All Speed Modes

Table 2. CJC5340 Mode Control

Operation as a Clock Master

As a clock master, LRCK and SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 18.

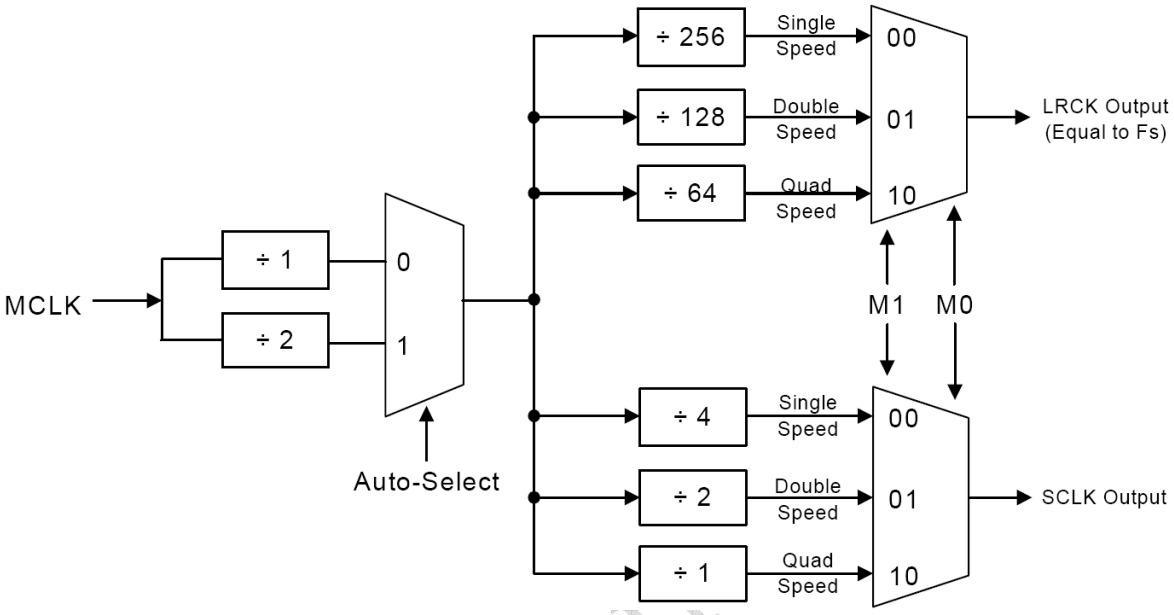


Figure 18. CJC5340 Master Mode Clocking

Operation as a Clock Slave with Auto-Detect

LRCK and SCLK operate as inputs in clock slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance.

A unique feature of the CJC5340 is the automatic selection of either Single-, Double- or Quad-Speed mode when operating as a clock slave. The auto-mode select feature negates the need to configure the Mode pins to correspond to the desired mode. The auto-mode selection feature supports all standard audio sample rates from 2 to 200 kHz. However, there are ranges of non-standard audio sample rates that are not supported when operating with a fast MCLK (512x, 256x, 128x for Single-, Double-, and Quad-Speed Modes, respectively). Please refer to Table for supported sample rate ranges.

Master Clock

The CJC5340 requires a Master clock (MCLK) which runs the internal sampling circuits and digital filters. There is also an internal MCLK divider which is automatically activated based on the speed mode and frequency of the MCLK. Table 3 shows a listing of the external MCLK/LRCK ratios that are required. Table 4 lists some common audio output sample rates and the required MCLK frequency. Please note that not all of the listed sample rates are supported when operating with a fast MCLK (512x, 256x, 128x for Single-, Double-, and Quad-Speed Modes, respectively).

	Single-Speed Mode	Double-Speed Mode	Quad-Speed Mode
MCLK/LRCK Ratio	256x, 512x	128x, 256x	64x*,128x
* Quad Speed, 64x only available in Master Mode.			

Table 3. Master Clock (MCLK) Ratios

SAMPLE RATE (kHz)	MCLK (MHz)
32	8.192
44.1	11.2896 22.5792
48	12.288 24.576
64	8.192
88.2	11.2896 22.5792
96	12.288 24.576
192	12.288 24.576

Table 4. Master Clock (MCLK) Frequencies for Standard Audio Sample Rates

Serial Audio Interface

The CJC5340 supports both I²S and Left-Justified serial audio formats. Upon start-up, the CJC5340 will detect the logic level on SDOUT (pin 4). A 10 kΩ pull-up to VL is needed to select I²S format, and a 10 kΩ pulldown to GND is needed to select Left-Justified format. Figures 19 and 20 illustrate the I²S and Left-Justified audio formats. Please see Figures 13 through 16, for more information on the required timing for the two serial audio interface formats. Also see Application Note AN282 for a detailed discussion of the serial audio interface formats.

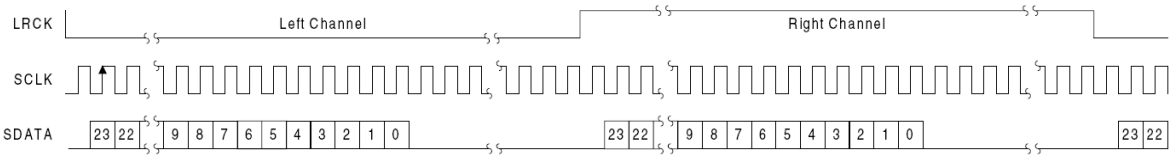


Figure 19. I²S Serial Audio Interface

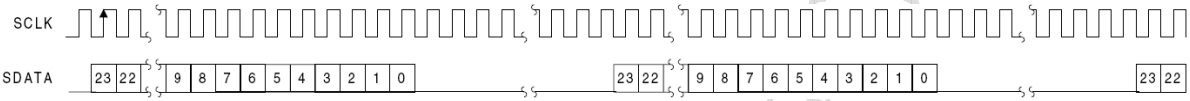


Figure 20. Left-Justified Serial Audio Interface

Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power-glitch-related issues.

Grounding and Power Supply Decoupling

As with any high-resolution converter, achieving optimal performance from the CJC5340 requires careful attention to power supply and grounding arrangements. Figure 17 shows the recommended power arrangements, with VA and VL connected to clean supplies. VD, which powers the digital filter, may be run from the system logic supply or may be powered from the analog supply via a resistor. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low-value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from FILT+ and
REF_GND. Furthermore, all ground pins on CJC5340 should be referenced to the same ground reference.

Synchronization of Multiple Devices

In systems where multiple ADCs are required, the user can achieve simultaneous sampling if the MCLK and LRCK signals are the same for all of the CJC5340's in the system. If only one master clock source is needed, one solution is to place one CJC5340 in Master mode, and slave all of the other CJC5340's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CJC5340 reset with the inactive (falling) edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

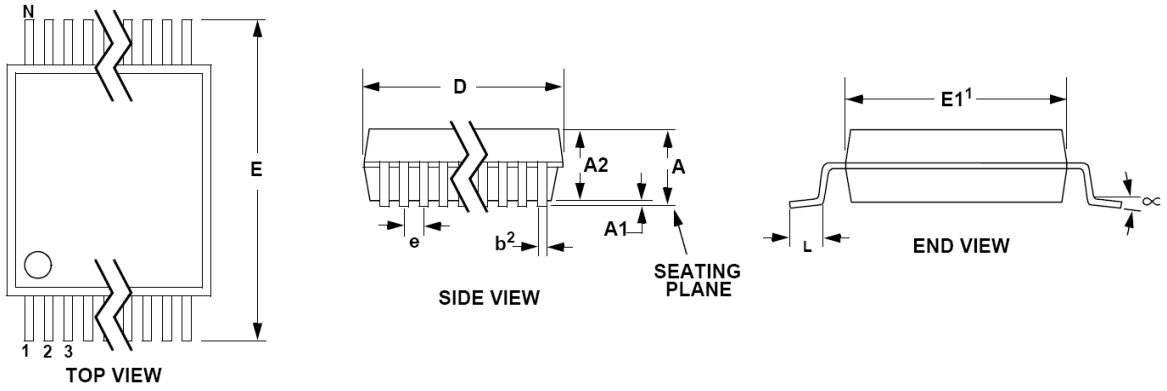
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

PACKAGE DIMENSIONS

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
μ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature		-	-	135	℃
Junction to Ambient Thermal Impedance	Θ_{JA}	-	75	-	℃/W